Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Previously Presented): A chip-size semiconductor package, comprising:

a semiconductor chip;

a metal pad formed on the semiconductor chip;

a conductive wiring pattern electrically connected to the metal pad;

a molding resin formed over the conductive wiring pattern; and

a terminal member which is electrically connected to the conductive wiring pattern, wherein

the conductive wiring pattern comprises a terminal portion on which the terminal member is formed, an extended portion extending from the terminal portion and a connecting portion arranged between the terminal portion and the extended portion,

the connecting portion has a width that gradually decreases toward the extended portion, and

the connecting portion has a slit to disperse stress applied to the connecting portion.

Claim 2 (Original): A chip-size semiconductor package according to claim 1, wherein

the connecting portion is provided with a plurality of slits, which are separated from each other.

Claim 3 (Previously Presented): A chip-size semiconductor package according to claim 2, wherein the slits are rectangular shaped and are arranged to extend radially away from each other.

Claim 4 (Canceled)

Claim 5 (Previously Presented): A chip-size semiconductor package, comprising:

a semiconductor chip;

a metal pad formed on the semiconductor chip;

a conductive wiring pattern electrically connected to the metal pad;

a molding resin formed over the conductive wiring pattern; and

a terminal member which is electrically connected to the conductive wiring pattern, wherein

the conductive wiring pattern comprises a terminal portion on which the terminal member is formed, an extended portion extending from the terminal portion and a connecting portion arranged between the terminal portion and the extended portion,

the connecting portion has a width that gradually decreases from a first boundary at the terminal portion to a second boundary at the extended portion, and

a dummy pattern arranged adjacent the first and second boundaries and along sides of the connecting portion, the molding resin also being formed on the dummy pattern.

Claim 6 (Previously Presented): A chip-size semiconductor package according to claim 5, wherein the dummy pattern is a conductive pattern which is formed during a same process as the conductive wiring pattern and is arranged parallel to the conductive wiring pattern.

Claim 7 (Previously Presented): A chip-size semiconductor package according to claim 5, wherein the dummy pattern comprises two parts respectively arranged along both sides of the connecting portion.

Claim 8 (Canceled)

Claim 9 (Currently Amended): A chip-size semiconductor package, comprising:

a semiconductor chip;

a metal pad formed on the semiconductor chip;

a conductive wiring pattern electrically connected to the metal pad;

a molding resin formed over the conductive wiring pattern; and

a terminal member which is electrically connected to the conductive wiring

pattern, wherein

the conductive wiring pattern comprises a terminal portion on which the terminal member is formed, an extended portion extending from the terminal portion and a connecting portion arranged between the terminal portion ~~and a connecting portion arranged between the terminal portion~~ and the extended portion,

the connecting portion has a width that gradually decreases from a first boundary at the terminal portion to a second boundary at the extended portion, and

a dent is formed at and around the connecting portion.

Claim 10 (Previously Presented): A chip-size semiconductor package according to claim 9, wherein the dent is square shaped.

Claim 11 (Canceled)

Claim 12 (Previously Presented): A chip-size semiconductor package, comprising:

a semiconductor chip;

a metal pad formed on the semiconductor chip;

a conductive wiring pattern electrically connected to the metal pad;

a molding resin formed over the conductive wiring pattern; and

a terminal member which is electrically connected to the conductive wiring pattern, wherein

the conductive wiring pattern comprises a terminal portion on which the terminal member is formed, an extended portion extending from the terminal portion and a connecting portion arranged between the terminal portion and the extended portion,

the connecting portion has a width that gradually decreases from a first boundary at the terminal portion to a second boundary at the extended portion, and

the connecting portion has a first region extending outwardly from the terminal portion and a second region extending in a perpendicular direction from the first region, the second region extending from the connecting portion.

Claim 13 (Previously Presented): A chip-size semiconductor package according to claim 12, further comprising a plurality of projecting parts each of which extends in the perpendicular direction from the conductive wiring pattern.

Claim 14 (Previously Presented): A chip-size semiconductor package according to claim 13, wherein the second region extends from both sides of the first region.

Claims 15-17 (Canceled)

Claim 18 (Previously Presented): A chip-size semiconductor package according to claim 1, further comprising a wafer coat formed over the semiconductor chip, wherein the conductive wiring pattern is formed on the wafer coat.

Claim 19 (Previously Presented): A chip-size semiconductor package according to claim 5, further comprising a wafer coat formed over the semiconductor chip, wherein the conductive wiring pattern is formed on the wafer coat.

Claim 20 (Previously Presented): A chip-size semiconductor package according to claim 9, further comprising a wafer coat formed over the semiconductor chip, wherein the conductive wiring pattern is formed on the wafer coat.

Claim 21 (Previously Presented): A chip-size semiconductor package according to claim 12, further comprising a wafer coat formed over the semiconductor chip, wherein the conductive wiring pattern is formed on the wafer coat.

Claim 22 (Previously Presented): A chip-size semiconductor package according to claim 1, wherein the terminal member comprises a conductive post that is arranged on the terminal portion, and a terminal that is formed on the conductive post and exposed from the molding resin.

Claim 23 (Previously Presented): A chip-size semiconductor package according to claim 5, wherein the terminal member comprises a conductive post that is arranged on the terminal portion, and a terminal that is formed on the conductive post and exposed from the molding resin.

Claim 24 (Previously Presented): A chip-size semiconductor package according to claim 9, wherein the terminal member comprises a conductive post that is arranged on the terminal portion, and a terminal that is formed on the conductive post and exposed from the molding resin.

Claim 25 (Previously Presented): A chip-size semiconductor package according to claim 12, wherein the terminal member comprises a conductive post that is arranged on the terminal portion, and a terminal that is formed on the conductive post and exposed from the molding resin.